EN0-001 Q&As

ARM Accredited engineer

Pass ARM EN0-001 Exam with 100% Guarantee

Free Download Real Questions & Answers **PDF** and **VCE** file from:

https://www.geekcert.com/en0-001.html

100% Passing Guarantee
100% Money Back Assurance

Following Questions and Answers are all new published by ARM Official Exam Center

QUESTION 1

Which instruction would be used to return from a Reset exception?

A. MOVS PC, R14

B. MOVSPC, R13

C. Architecturally not defined

D. SUBS PC, R14, #4

Correct Answer: C

QUESTION 2

What is the value of r0 after executing the following instruction sequence?

MOV r0, #200

MOV r5, #1

STR r3, [r0, r5, LSL#3]!

A. 200

B. 201

C. 204

D. 208

Correct Answer: D

QUESTION 3

In Architecture ARMv7-A which one of the following has a known physical address at power-on reset?

A. The exception vector table

B. The Memory Management Unit (MMU) translation table

C. The Stack Pointer (SP)

D. The System Control Register (SCTLR)

Correct Answer: A

QUESTION 4

A simple system comprises of the following memory map:

Flash - 0x0 to 0x7FFF

RAM - 0x10000 to 0X17FFF

When conforming to the ABI, which of the following is a suitable initial value for the stack pointer?

A. Top address of RAM (0x18000)

B. Top address of flash (0x8000)

C. Bottom address of RAM (0x10000)

D. Bottom address of flash (0x0000)

Correct Answer: A

QUESTION 5

An interrupt handler contains the following instruction sequence at the end. The purpose of these instructions is to clear the interrupt request in the interrupt controller and then safely re-enable interrupts.

STR r0, [r1] ; write to interrupt controller register to clear interrupt request

CPSIE i ; re-enable IRQ interrupts Which of the following instructions should be placed at position in order to ensure that the interrupt

controller sees the write before interrupts are re-enabled?

A. DMB

B. DSB

C. ISB

D. NOP

Correct Answer: B