EN0-001 Q&As

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QUESTION 1

In an ARMv7-A processor that includes the Advanced SIMD extension (NEON), where are the data values operated on by NEON instructions stored?

A. In system memory

B. In registers shared with the VFP register set

C. In registers shared with the integer register set

D. In dedicated registers not shared with other registers

Correct Answer: B

QUESTION 2

Which one of the following statements best describes the function of vector catch logic?

A. It traps writes to the memory containing the vector table

B. It provides additional resources for debugging exception handlers

C. It provides configurable exception priorities on an ARM processor

D. It provides an improved mechanism for an application to handle exceptions

Correct Answer: B

QUESTION 3

On a processor supporting the Security Extensions, what sequence of operations is required to move from Non-secure User mode to Secure state?

A. This transition is not possible

B. Execution of an SMC instruction

C. Execution of an SMC instruction followed by an SVC instruction

D. Execution of an SVC instruction followed by an SMC instruction

Correct Answer: D

QUESTION 4

Which one of the following statements is TRUE for software breakpoints?

A. Limited software breakpoints can be placed in code running from ROM

B. Each software breakpoint requires one watchpoint resource in the debug hardware

C. Each software breakpoint requires one breakpoint resource in the debug hardware

D. The number of available software breakpoints is not limited by the debug hardware

Correct Answer: D

QUESTION 5

In an ARMv7-A processor with Security Extensions, which of the following mechanisms best describes the way Secure memory is protected from access by software running in a Non-secure privileged mode?

A. The memory system has visibility of the security status of all accesses, and will reject all Non- secure accesses to Secure memory

B. Secure memory contents are encrypted, and cannot be decrypted by Non-secure software

C. The level 2 cache controller blocks all accesses to Secure memory when the SCR.NS bit of the processor is set

D. The MMU generates an abort on accesses to Secure memory performed by Non-secure software

Correct Answer: A