EN0-001 Q&As

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QUESTION 1

Using a lower optimization level when compiling will:

A. Produce faster code.

B. Produce smaller code.

C. Produce non standard-compliant code.

D. Produce code that might be easier to debug.

Correct Answer: D

QUESTION 2

An Advanced SIMD intrinsic has the prototype:

uint8xl6x2_t vld2q_u8 (uint8_t const * ptr);

How many bytes does this intrinsic load from memory?

A. 2

B. 16

C. 32

D. 256

Correct Answer: C

QUESTION 3

Implementing loops using a decrementing counter which exits the loop when a counter reaches zero can be beneficial for power and performance. This is because:

A. A simpler branch instruction can be used.

B. Decrementing variables uses less power than incrementing them.

C. The decrement and branch operations can be encoded as a single instruction.

D. The loop termination condition check can be integrated into the subtract operation.

Correct Answer: D

QUESTION 4

Consider a sequence of five independent instructions running on a pipelined processor. There are no interlocks and no data dependencies between instructions, and each instruction takes one cycle to execute. The processor has three pipeline stages and is not superscalar.

How many cycles does it take to fetch, decode and execute all five instructions in sequence, assuming that there are no pipeline stalls?

A. 5 cycles

B. 7 cycles

C. 8 cycles

D. 15 cycles

Correct Answer: B

QUESTION 5

When using the Performance Monitoring Unit to count runtime events the counter registers are limited to 32-bits. How can more than 2A32 events be counted without significantly impacting the software performance?

A. Register an interrupt which is triggered when the counter overflows

B. Count the events using a 64-bit VFP register

C. Allow one event type to use concatenated counter registers

D. Poll the event counter, resetting it when the counter is close to overflowing

Correct Answer: A