EN0-001 Q&As

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QUESTION 1

For Cortex-A series cores, what instruction(s) are recommended to implement a mutex or semaphore?

A. SWP and SWPB

B. DSB and ISB

C. LDREX and STREX

D. DMB

Correct Answer: C

QUESTION 2

A Programmer\\'s View CPU model usually provides:

A. Cycle-accurate simulation of the CPU.

B. Instruction-accurate simulation of the CPU.

C. Simulation of user-defined memory-mapped peripherals.

D. Cycle-accurate simulation of the cache and memory system.

Correct Answer: B

QUESTION 3

Assume a multicore processor with coherency management based on the MESI protocol. When a core changes the contents of a shared cache line, what is the final status of that line in the local cache?

A. Modified

B. Exclusive

C. Shared

D. Invalid

Correct Answer: A

QUESTION 4

A C code segment contains three calls to a function, foobar ().

This code segment is to be linked with a static library that defines foobar ().

Ignoring inlining, how many copies of foobar () will the ARM linker place in the output?

A. None

B. Always one

C. Always three

D. One or more depending on optimization level

Correct Answer: B

QUESTION 5

Which one of these statements is TRUE about code running on final hardware without a debugger attached?

A. FIQ exceptions must not be taken

B. The instruction cache must be enabled

C. Global variables must be initialized to zero

D. The Reset Vector must reside in non-volatile memory

Correct Answer: D